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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/732,700	12/11/2000	Shinya Udo	024014-00001	2922

7590 05/18/2004

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EXAMINER	
ANYASO, UCHENDU O	
ART UNIT	**PAPER NUMBER**
2675	14

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/732,700	UDO ET AL.	
	Examiner	Art Unit	
	Uchendu O Anyaso	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. **Claims 1-11** are pending in this action.

Claim Rejections - 35 USC ' 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 1-11** are rejected under 35 U.S.C. 103(a) as being unpatentable over *Takita et al* (U.S. 6,151,005) in view of Yanagi et al (U.S. 6,310,616), and further in view of *Johnson* (U.S. 5,625,373).

Regarding **independent claim 1**, and for **claim 11**, Takita teaches an X-driver circuit (100) which delivers a voltage corresponding to the display data to each data line of the liquid crystal panel (column 5, lines 25-34, figures 1, 2 at 100).

Furthermore, Takita teaches a grayscale voltage generating portion by teaching voltage divider circuits (120-0, 206) by which a voltage across the outputs (204, 205) is divided into voltages of 16 levels (column 11, lines 44-60, figure 2 at 120-0, 204-206; *see also* column 12, lines 14-37, figure 2 at 120-0, 204-206).

Also, Takita teaches a selector portion for each of the data bus lines and selecting any one of the plurality of analog grayscale voltages based on the grayscale data by teaching an X driver circuit into which display data to be displayed on a liquid-crystal panel is supplied, and which delivers a voltage corresponding to the display data to each data line of the liquid-crystal panel;

may well comprise a voltage divider circuit provided for each data line, by which n voltages externally supplied are divided into m voltages (n<m) corresponding to the display data; the voltage divider circuit including a first selector circuit which is supplied with the n unequal voltages, and which selects and delivers two of the supplied n voltages; a first control circuit which controls the first selector circuit in accordance with the display data so as to select the two voltages; an output circuit which can deliver either of a plurality of divisional voltages produced from the selected voltages, and the supplied voltages; a second selector circuit which selects and delivers any of the plurality of divisional voltages and the supplied voltages; and a second control circuit which controls the second selector circuit under either of a voltage selection command externally supplied and a voltage selection command internally generated, so as to select the voltage to-be-delivered from either of the supplied voltages and the plurality of divisional voltages corresponding to the display data; the voltage selection command being a command for selecting a higher one of the two voltages selected by the first selector circuit, during a first period, while it is a command for selecting the divisional voltage corresponding to the display data, during a second period subsequent to the first period. (column 5, lines 25-52).

Furthermore, Takita teaches a plurality of grayscale voltages connected to the grayscale (V0-V4) that supplies the grayscale voltages to the selector portion (201) (figure 2 at V0-V4, 201).

However, Takita does not teach a switching portion for electrically connecting and disconnecting a plurality of grayscale voltage lines from a grayscale voltage generating portion. On the other hand, Yanagi teaches a drive circuit for a display device that supplies a plurality of grayscale voltages to the display device (*see* Abstract) comprising capacitors (C1, C2) and

switching portions (SW_{11}, SW_{12}, SW_{21}, SW_{22}) that enable connecting and disconnecting a plurality of grayscale voltage lines from a grayscale voltage generating circuit P4 (column 38, lines 21-54, figure 31 at 12a, 12b, C_1, C_2, SW_{11}, SW_{12}, SW_{21}, SW_{22}).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Takita and Yanagi's inventions because while Takita teaches an X-driver circuit (100) which delivers a voltage corresponding to the display data to each data line of the liquid crystal panel (column 5, lines 25-34, figures 1, 2 at 100) with switching portions (202, 203) that delivers high and low potentials on the output bus (column 11, lines 63-67 through column 12, lines 1-2, figure 2 at 202, 203), Yanagi teaches capacitors and switching portions for electrically connecting and disconnecting a plurality of grayscale voltage lines from a grayscale voltage generating portion P4 (*see* column 38, lines 21-54, figure 31 at 12a, 12b, C_1, C_2, SW_{11}-SW_{22}; *see also* column 15, lines 20-36). The motivation for combining these inventions would have been to design a high-grade display device with low power consumption (column 16, lines 17-27).

However, Takita and Yanagi do not teach how these switching circuits are used during an operation test. On the other hand, Johnson teaches an invention for conducting operation tests in a flat panel display in order to eliminate visual anomalies wherein an error measurement device (22) is connected to a selector switch (12) that provides electrical connection to each column driver (column 3, lines 55-67; column 7, lines 24-30, figures 3, 6 at 12, 22).

Thus, it would have been obvious to a person of ordinary skill in the art to combine Takita, Yanagi, and Johnson because while the combination of Takita and Yanagi teach a display device that supplies a plurality of grayscale voltages to the display device comprising capacitors and switching portions that enable connecting and disconnecting a plurality of grayscale voltage

lines from a grayscale voltage generating circuit P4, Johnson teaches an invention for conducting operation tests in a display device in order to eliminate visual anomalies wherein an error measurement device (22) is connected to a selector switch (12) that provides electrical connection to each column driver (column 3, lines 55-67; column 7, lines 24-30, figures 3, 6 at 12, 22). The motivation for combining these inventions would have been to eliminate any sought of visual anomalies that may appear in a display system (column 1, lines 4-6).

Regarding **claims 2** and **3**, in further discussion of claim 1, Takita teaches a voltage generating portion (206) that has a ladder resistor portion with a plurality of resistors connected in series and which generates a plurality of analog grayscale voltages through resistance divisions (figure 2 at 206).

Regarding **claims 4-8**, in further discussion of claim 1, Takita teaches switching portions (202, 203) that delivers high and low potentials on the output bus (column 11, lines 63-67 through column 12, lines 1-2, figure 2 at 202, 203).

Regarding **claims 9** and **10**, in further discussion of claim 4, Johnson teaches an invention for conducting operation tests in a flat panel display in order to eliminate visual anomalies wherein an error measurement device (22) is connected to a selector switch (12) that provides electrical connection to each column driver (column 3, lines 55-67; column 7, lines 24-30, figures 3, 6 at 12, 22).

Response to Arguments

4. Applicant's arguments filed March 1, 2004 have been fully considered but they are not persuasive.

In applicant's Remarks, applicant argues that Yanagi does not disclose or suggest a switching portion electrically disconnecting the plurality of grayscale voltage lines from the grayscale voltage generating portion during an operation test and electrically connecting the plurality of grayscale voltage lines to the grayscale voltage generating portion during a normal mode of operation. Applicant contends that the switches (SW11, SW12, SW21, SW22) of the grayscale voltage generating circuit P4 merely enable connecting and disconnecting the capacitors C1 and C2 from the power supply circuits 12a and 12b.

Examiner disagrees with Applicant's contentions because a complete reading of Yanagi shows that the **gray-scale voltage generating circuit P4** is characterized in that a pair of gray-scale power supply circuits 12a and 12b which respectively output the external gray-scale voltages v0 and v2 are provided wherein a power supply circuit with a structure similar to that of the gray-scale voltage generating circuit P4 may be provided between each pair of external gray-scale voltages v0, v2 ; v2, v5 ; v5, v7 which is required for forming the gray-scale voltages v1 ; v3, v4 ; and v6 (column 38, lines 21-38, figure 31).

Furthermore, the gray-scale voltage generating circuit P4 corresponds to a pair of external gray-scale power supplies V0 and V2 among pairs of the external gray-scale power supplies V0, V2 ; V2, V5 ; V.sub.5, V.sub.7 wherein the capacitors C1 and C2 are connected to or disconnected from the power supply circuit at the same time with the switching between a positive level and a negative level of the output voltage from the power supply circuit such that

the disconnection is conducted right before the switching and the connection is conducted when an appropriate period of time elapses after the switching; more specifically, the connection is conducted after a transition period following the switching (column 38, lines 38-54, figure 31).

The relationship among the grayscale voltage generating circuit P4, power supply circuits 12a, 12b, and the grayscale voltages v1-v7 is the key to understanding how Yanagi reads on the features of applicant's claim 1.

As such, Yanagi does indeed teach how the switching portion of the voltage generating circuit P4 electrically disconnects and connects to the grayscale voltage lines. Hence, by combining Takita, Yanagi and Johnson we are able to achieve a design that highlights a switching portion electrically disconnecting the plurality of grayscale voltage lines from the grayscale voltage generating portion during an operation test and electrically connecting the plurality of grayscale voltage lines to the grayscale voltage generating portion during a normal mode of operation. This is because it would have been obvious to a person of ordinary skill in the art to combine Takita, Yanagi, and Johnson because while the combination of Takita and Yanagi teach a display device that supplies a plurality of grayscale voltages to the display device comprising capacitors and switching portions that enable connecting and disconnecting a plurality of grayscale voltage lines from a grayscale voltage generating circuit P4, Johnson teaches an invention for conducting operation tests in a display device in order to eliminate visual anomalies wherein an error measurement device (22) is connected to a selector switch (12) that provides electrical connection to each column driver (column 3, lines 55-67; column 7, lines 24-30, figures 3, 6 at 12, 22). The motivation for combining these inventions would have been

to eliminate any sought of visual anomalies that may appear in a display system (column 1, lines 4-6).

Therefore, applicant's arguments are not persuasive.

Conclusion

5. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Uchendu O. Anyaso whose telephone number is (703) 306-5934. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve Saras, can be reached at (703) 305-9720.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Uchendu O. Anyaso

05/14/2004

CHANH NGUYEN
PRIMARY EXAMINER